REMARKS

In the Office Action dated February 26, 2004, claims 21-33 were rejected under 35 U.S.C. § 112, ¶ 2; and claims 1-13 and 16-21 were rejected under § 103 over U.S. Patent No. 6,092,156 (Schibinger) in view of U.S. Patent No. 6,356,983 (Parks).

Applicant acknowledges the indication that claims 14, 15, and 22-33 would be allowable if informalities were addressed.

Claims 12, 16, 22, and 31 have been amended to improve their form. The scope of each of the claims has not been changed.

REJECTION UNDER 35 U.S.C. § 112, ¶ 2

Claim 21 has been amended by deleting the term "to the first memory controller" at line 8. This amendment removes the antecedent basis problem noted in the Office Action. Note that this amendment has *broadened* the scope of claim 21.

The remaining amendments of claim 21 are made to improve form and do not change the scope of the claim.

REJECTION UNDER 35 U.S.C. § 103

To establish a *prima facie* case of obviousness, a first requirement is that there must be some motivation or suggestion to combine the reference teachings. *See* MPEP § 2143 (8th ed., Rev. 1) at 2100-124,125. A second requirement of a *prima facie* case is that references when combined must teach and suggest *all* elements of the claim. *See id.* at 2100-125. In the present case, neither requirement of a *prima facie* case of obviousness has been established with respect to claim 1.

The Office Action conceded that Schibinger does not disclose the last clause of claim 1, namely "allowing access to a second memory location of the shared memory to the second processor while the first processor has exclusive access to the first memory location." Instead, the Office Action relied upon Parks as disclosing this feature. However, Applicant notes that there is no motivation or suggestion to combine Schibinger and Parks as proposed by the Office Action. Schibinger actually *teaches away* from the claimed invention. Schibinger describes a system that avoids deadlocks when performing non-atomic operations on data in a shared memory accessed by

multiple processors. Schibinger, Abstract. The Schibinger system includes memory storage units 110 (Figure 1 of Schibinger) and processing modules 120 that contain three levels of caches (*see* Figure 5 of Schibinger). A coherency scheme is defined that allows for only one requestor to have exclusive ownership at a time of a cache line. Schibinger, 7:50-55. Also, to avoid a deadlock situation in a non-atomic operation, a processor is able to issue a split lock request to a third level cache that corresponds to the processor. Schibinger, 8:30-31. Note that multiple third level caches are part of the system, with each third level cache coupled to respective processors (*see* Figure 5 of Schibinger), and each third level cache to submit requests to the memory modules on behalf of the processors. In response to a split lock request from the processor, a third level cache generates a lock message that is transmitted to a memory storage unit 110. Schibinger, 8:35-37. In response, the memory storage unit 110 sends a grant message back to the multiple third level caches. Schibinger, 8:37-38. This grant message is targeted for only one of the third level caches 510. All third level caches that are not granted generate a "gone idle" message, which is used by the particular third level cache performing this split lock operation to ensure that *all other third level caches cannot access memory*. Schibinger, 8:41-45. Therefore, Schibinger explicitly teaches that while one processor has exclusive access of shared memory (memory storage unit 110 in Schibinger), other processors will not be able to issue a request to the memory through respective third level caches.

Thus, it is clear that Schibinger teaches away from the subject matter of claim 1, which recites *allowing access* to a second memory location of the shared memory to the second processor while the first processor has exclusive access to the first memory location. As noted by the MPEP, "prior art must be considered in its entirety, including disclosures that teach away from the claims." MPEP § 2145 at 2100-156. Since Schibinger teaches away from the claimed invention, that is a strong indication that there is no motivation or suggestion to combine Schibinger with Parks in the manner proposed by the Office Action. Thus, for at least this reason, a *prima facie* case of obviousness has not been established with respect to claim 1.

In addition, even if Schibinger and Parks can be combined, the hypothetical combination of the references does not teach or suggest *all* elements of claim 1. The

Office Action contended that Parks discloses the allowing act of claim 1. Parks describes a multiprocessor system having a shared memory, plural processor nodes, and a cache implemented within at least some of the processor nodes, with a state machine associated with each memory location to indicate various states. Parks, 4:8-22. The various states are part of a cache coherency scheme. One of the issues addressed by Parks is how exclusive access over a cache line can be transitioned from one processor to another processor. Parks, 13:26-29. Parks describes a "conventional" directory-based protocol in which a first processor has exclusive control over a cache line. If a second processor desires exclusive control such cache line, the cache line state must first transition from exclusive to uncached or shared, followed by a message that is sent to the second processor that the cache line is now available. Parks, 13:29-37. What this aspect of Parks teaches is that another processor cannot obtain exclusive control of a cache line until the state of the cache line has transitioned from the exclusive state to a non-exclusive state. There is no teaching in Parks of allowing the second processor access to a second memory location of a shared memory while the first processor has exclusive access to a first memory location of the shared memory. Instead, Parks teaches that exclusive control of a cache line is transitioned from one processor to another processor. Therefore, even if Schibinger and Parks can be properly combined, the hypothetical combination of the references does not teach or suggest each and every element of claim 1. For this additional reason, a *prima facie* case of obviousness has not been established with respect to claim 1.

A *prima facie* case of obviousness has also not been established with respect to independent claims 10 and 21 for reasons similar to those in claim 1. All dependent claims (including newly added dependent claims 34-36) are allowable over the cited references for at least the same reasons as corresponding independent claims.

Moreover, with respect to dependent claim 4, neither Schibinger nor Parks discloses or suggests that the requesting exclusive access act further comprises forwarding a lock request from a memory controller to a switch. The Office Action conceded that Parks does not disclose forwarding a lock request from a memory controller to a switch. However, the Office Action stated that "it is notoriously well know [sic] in the art that the memory is comprising a controller or control logic to

response [sic] a request from/to the requesting processor." 2/26/2004 Office Action at 4. Such knowledge, even assuming it is "notoriously well known" does not constitute "forwarding the lock request from the memory controller to a switch," as recited in claim 4. Moreover, the Office Action has cited to no reference that establishes that forwarding a lock request from the memory controller to a switch, *in the context of claim 4*, would be well known. If such a reference exists, Applicant requests the production of such reference. Otherwise, withdrawal of the rejection of claim 4 is respectfully requested.

With respect to dependent claim 6, the Office Action cited to table 5, column 13, line 50, through column 14, line 16, of Parks as disclosing the feature of claim 6. Table 5 of Parks does not disclose or suggest saving a lock request information if a memory location is not currently assigned, and sending the lock request information to a memory controller, as recited in claim 6.

With respect to dependent claim 11, which depends from claim 10, the Office Action cited to Schibinger as disclosing the act of forwarding the lock request from a first memory controller to a switch. The Office Action pointed to the crossbar 350 shown in Figure 3 of Schibinger as the switch. However, note that the crossbar 350 is part of the processing module 120, and that lock requests are sent from a subprocessing module 310 to the crossbar 350 (*see* Figure 3 of Schibinger). Therefore, in Schibinger, a lock request is *not* forwarded from a memory controller (which is in the memory storage unit 110) to a switch (rather, lock requests are sent by a processor to the crossbar 350). In view of the foregoing, a *prima facie* case of obviousness has not been established with respect to dependent claim 11.

Similarly, with respect to dependent claim 16, the hypothetical combination of Schibinger and Parks fails to disclose or suggest forwarding a lock request from a first memory controller to a switch.

With respect to dependent claim 18, the Office referred to the rejection of claims 5 and 6. However, note that claim 18 recites "broadcasting the lock request information to each memory controller of each of the plurality of multiprocessor nodes." This element is not recited in claims 5 or 6. Furthermore, the broadcasting act of claim 18 is not taught or suggested by either Schibinger or Parks. Therefore, a *prima facie* case of obviousness has not been established with respect to claim 18.

With respect to new claim 34, which depends from claim 1, the hypothetical combination of Schibinger and Parks fails to disclose or suggest *forwarding* a lock request from a memory controller to a switch, and the switch *broadcasting* lock request information to the first memory controller and at least another memory controller.

In view of the foregoing, all claims are in condition for allowance, which action is respectfully requested. The Commissioner is authorized to charge any additional fees, including extension of time fees, and/or credit any overpayment to Deposit Account No. 08-2025 (200301872-1).

Respectfully submitted,

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